SGS-THOMSON MICROELECTRONICS

QN109
QUALITY NOTE

NEW METALISATION SCHEME FOR EPROMS WITH UPGRADED PROCESS

Over the last few years SGS-THOMSON has been continuously upgrading the process technology of its EPROM products. This upgrading has taken the form of improved process technology, improved designs and smaller chip sizes. Giving improvements in cost, quality and performance of the products.

The CMOS E5-U35 is a third upgrade of the original CMOS E5 0.8 µm process with a more compact layout and a new 15% shrink of some of the circuits dimensions.(See Reference PCN MPG/NV94-01). To obtain this higher density device some of the process steps have been improved.

It is well known that Aluminium interconnection lines containing copper have a high electromigration resistance as the copper acts as an "hillocks suppression agent"(See Reference 1 & 2). Using aluminium lines alloyed with 0.5% copper by weight, experiments show that the redistribution of copper atoms at the grain boundaries and the formation of aluminium/copper chemical bonds at grain boundaries makes the boundaries resistant to the diffusion of aluminium atoms.

This is why a three layer metallization system of:

– 500Å Titanium / 1000Å Titanium Nitride
– 500Å Titanium
– 5300Å Aluminium / 1% Silicon / 0.5% copper

followed by 325Å Titanium Nitride as an antireflective coating has been chosen for the new CMOS E5-U35 process.

The first layer of Titanium/Titanium Nitride is needed to assure low contact resistivity and as an adhesion promoter for the tungsten plug used in the E5-U35 contacts. (see cross sectional representation Figure 2). The second layer of pure Titanium of 500Å is needed to assure good adhesion of the Aluminium alloy. The final Titanium Nitride layer deposited on the Aluminium alloy is used as an antireflecting coating to minimize light scattering during the metallization patterning process for the very high density metallization stripes.

This type of metallization system has been studied and is being introduced by many of the high density memory manufactores (Reference 1), but to assure its effectiveness SGS-THOMSON has performed an FMEA (Failure Mode and Effect Analysis) to validate the new metallization system. The major potential failure modes such as interconnection resistance change, electromigration, corrosion and wire bond weakness have been considered and evaluated.

The new metallization system can be easly extended (without process modification) also to the previous upgrades of CMOS E5, that is the U10 and U20, because it is considered to be an optimization of the metallization and metallization etching process and contributes to the process harmonization between the older process upgrade versions and the new one.

Tungsten plug technology for contact filling, used for CMOS E5 U35,is not extended to the older upgrades since it is considered to be not critical for their contact hole dimensions and such a process extension is not feasible without a Tungsten plug optimization for the old contact structures.

The final structure of the new metallization systems for CMOS E5-U35 and CMOS E5-U10 and E5-U20 will be according to the schemes shown in Figures 1 & 2.

Figure 1. CMOS E5 U10/U20 Cross Section

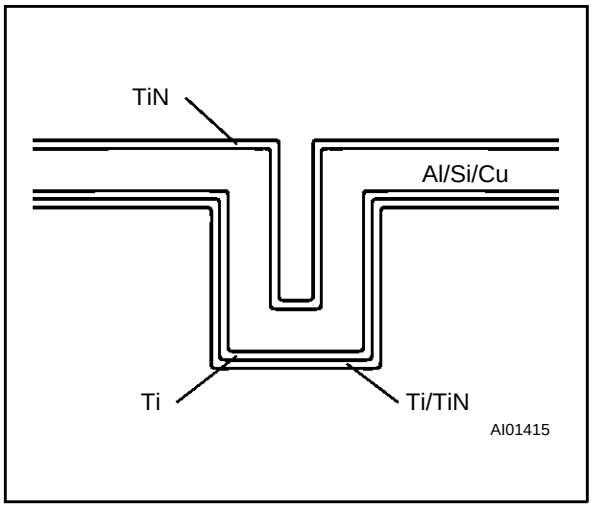
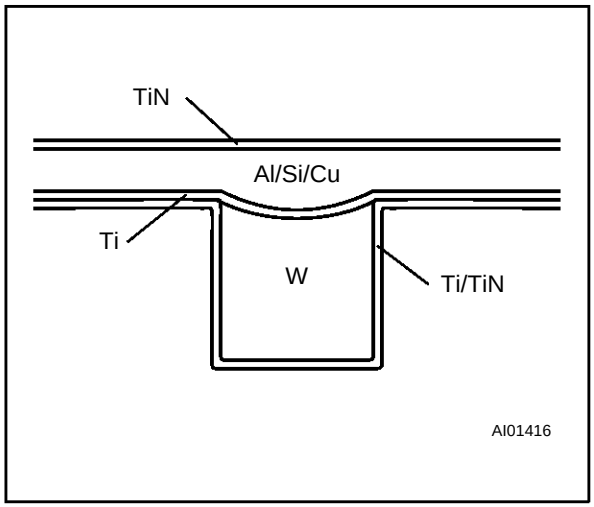


Figure 2. CMOS E5 U35 Cross Section



Reference:

(1) Carol D. Graas, Huy A. Lee, W McPherson, Robert H. Havemann "Electromigration reliability improvement of W plug vias with Ti layering" IRPS Vol.32 pp 173-177, 1994

(2) Takenao Nemoto and Takeshi Nogami "Segregation of Cu to grain boundaries by aging treatment and its effect on electromigration resistance for AlCu/TiN lines" IRPS Vol.32 pp 207-212, 1994